Please replace the last paragraph bridging pages 3 and 4 with the following rewritten paragraph:

--This crystal oscillator is constructed as follows. As illustrated in Fig. 7, between an input terminal and an output terminal of an inverter amplifier 101 there is inserted a parallel circuit comprised of a crystal resonator 102 and a feedback resistor R1. Additionally, a capacitor C2 is connected to the output terminal of the inverter amplifier 101, and a MOS construction type capacitance element 103 is connected to the input terminal of the inverter amplifier. And, simultaneously, an electric-charge injection terminal TI of the MOS construction type capacitance element 103 and a control terminal Vcont are connected to each other.--

Please replace age 4, first full paragraph, with the following rewritten paragraph:

--As the MOS construction type capacitance element 103, although it is only a mere one example, there is known the one illustrated in Fig. 8. Namely, in this element 103, a positive or negative voltage is applied to the control terminal Vcont by using the N type substrate as a basis to thereby cause the flow of a tunnel current through the interior of SiO_2 to thereby cause electrons to inject into or come out of a floating electrode 104.--

Please replace the last paragraph bridging pages 4 and 5 with the following rewritten paragraph:

--However, as will be explained below, fundamentally, the MOS construction type capacitance element can have its capacitance value varied over a wide range only with use of a positive power supply or negative power supply. For this reason, there was the drawback that almost no change in the capacitance value occurred when merely using only either a positive, or a negative, single-polarity power supply alone.--

Please replace page 5, second full paragraph, with the following rewritten paragraph:

--Fig. 9 is a graph illustrating an example of the relationship between an inter-electrode voltage and a capacitance value of the MOS construction type capacitance element.--

Please replace page 5, fifth full paragraph, with the following rewritten paragraph:

--Accordingly, in the case of the crystal oscillator such as that illustrated in Fig. 7, in order to obtain a wide range of variable capacitance with use of the MOS construction type capacitance element 103, it is necessary to use control voltage sources for applying both positive and negative voltages to the control terminal Vcont. Therefore, there was the problem that the construction of the system making control of the frequency became complex.--

Please replace page 6, first full paragraph, with the following rewritten paragraph:

--The present invention has been made in order to solve the above-described problems and has an object to provide a small-sized piezoelectric oscillator which, while using a MOS construction type capacitance element suited to conversion to an IC version, enables obtaining a wide range of changes in the variable capacitance even with use of either a positive, or a negative, single-polarity power supply, and which facilitates the frequency control.--

Please replace page 6, second full paragraph, with the following rewritten paragraph:

--To attain the above object, according to the first aspect of the invention, there is provided a piezoelectric oscillator wherein, in an oscillator including a piezoelectric resonator, an amplifier, and a variable-capacitance element, the variable-capacitance element is a MOS construction type capacitance element, one terminal of that is applied with an alternating current voltage, whose intermediate voltage is a V voltage, and the other terminal of that is applied with a control voltage falling within a range whose intermediate value is the V voltage.--

Please replace the last paragraph bridging pages 6 and 7 with the following rewritten paragraph:

--According to the second aspect of the invention, there is provided a piezoelectric oscillator wherein, in an inverter piezoelectric oscillator in which a piezoelectric resonator is connected between an input terminal and an output terminal of an inverter amplifier; and divisional capacitors C1 and C2 are connected between respective ends of the piezoelectric resonator and the ground, by inserting a MOS construction type capacitance element in series with the piezoelectric resonator, one end of the MOS construction type capacitance element is applied with a bias voltage which is the V voltage at an output end or input end of the inverter

amplifier and the other end thereof has supplied thereto a control voltage that varies within a range whose intermediate value is the V voltage.--

Please replace page 7, first full paragraph, with the following rewritten paragraph:

--According to the third aspect of the invention, there is provided a piezoelectric oscillator wherein, in an inverter piezoelectric oscillator in which a piezoelectric resonator is connected between an input terminal and an output terminal of an inverter amplifier; and divisional capacitors C1 and C2 are connected between respective ends of the piezoelectric resonator and the ground, two MOS construction type capacitance elements are inserted respectively on both sides of the piezoelectric resonator; one end of each of the MOS construction type capacitance elements is applied with an alternating current voltage, whose intermediate voltage is a V voltage; and the other end thereof is applied with a control voltage that varies within a range whose intermediate value is the V voltage.--

A1 (cont'd)

Please replace the last paragraph bridging pages 7 and 8 with the following rewritten paragraph:

--According to the fourth aspect of the invention, there is provided a piezoelectric oscillator wherein, in an inverter oscillator in which a piezoelectric element is connected to an input or output end of an inverter amplifier; and divisional capacitors C1 and C2 are connected between respective ends of the piezoelectric element and the ground, a MOS construction type capacitance element is inserted between the piezoelectric resonator and an input end of the inverter amplifier or between the piezoelectric resonator and an output end of the inverter amplifier; a control voltage Vcont is applied to the terminal on a connection-to-piezoelectric resonator side of the MOS construction type capacitance element; and, when it is assumed that V represents the voltage that is a direct current bias voltage at the input end or output end of the inverter amplifier and that is applied to one end of the MOS construction type capacitance element, it is arranged that said voltage becomes an intermediate voltage of the control voltage Vcont.--

Please replace page 8, first full paragraph, with the following rewritten paragraph:

--According to the fifth aspect of the invention, there is provided a piezoelectric oscillator wherein, in an inverter oscillator in which a piezoelectric element is connected to an input or output end of an inverter amplifier; and divisional capacitors C1 and C2 are connected between respective ends of the piezoelectric element and the ground, a MOS construction type capacitance element is inserted between the piezoelectric resonator and an input end of the inverter amplifier or between the piezoelectric resonator and an output end of the inverter amplifier and a control voltage Vcont is applied to the terminal on the connection-to-piezoelectric resonator side of the MOS construction type capacitance element; a direct current circuit of a resistor and a capacitor is inserted and connected between the terminal on the inverter-amplifier side of the MOS construction type capacitance element and the input or output terminal of the inverter amplifier; and further a direct current bias voltage is applied to the terminal on the inverter-amplifier side of the MOS construction type capacitance element.--

A7 (Cont'd)

Please replace the last paragraph bridging pages 8 and 9 with the following rewritten paragraph:

--According to the sixth aspect of the invention, there is provided a piezoelectric oscillator according to the fifth aspect of the invention, wherein the amplitude level of an alternating current supplied to the MOS construction type capacitance element is adjusted according to the value of the resistance of the direct current circuit; and when it is assumed that V represents the direct current bias voltage supplied to the terminal on the inverter-amplifier side of the MOS construction type capacitance element, it is arranged that the direct current bias voltage V becomes an intermediate voltage of the control voltage Vcont.--

Please replace page 10, fourth full paragraph, with the following rewritten paragraph:

--Fig. 7 is a circuit diagram illustrating a conventional crystal oscillator using a MOS construction type capacitance element;--

A8

Please replace page 10, fifth full paragraph, with the following rewritten paragraph:

--Fig. 8 is a view of a sectional structure of the MOS construction type capacitance element; and--

Please replace page 10, sixth full paragraph, with the following rewritten paragraph:

--Fig. 9 illustrates the relationship between a terminal-to-terminal voltage and a capacitance value of the MOS construction type capacitance element.--

Please replace the last paragraph bridging pages 10 and 11 with the following rewritten paragraph:

--The crystal oscillator illustrated in Fig. 1 has the following construction. Between input and output terminals of an inverter amplifier 1, whose power source voltage is Vcc, there are respectively inserted in parallel a feedback resistor R1 and a series circuit consisting of a crystal resonator 2 and a resistor R2. And, between the input terminal of the inverter amplifier 1 and the ground there is inserted a capacitor C1 while, on the other hand, between one end of the crystal resonator 2 and the ground there is inserted a capacitor C2. Further, between the other end of the crystal resonator 2 and the ground there is grounded via a capacitor C3 a MOS construction type capacitance element 3 while, on the other hand, a point of connection between the MOS construction type capacitance element 3 and the capacitor C3 is connected to a control terminal Vcont via a resistor R3.--

Please replace page 11, third full paragraph, with the following rewritten paragraph:

--As apparent from the above-described explanation as well, the crystal oscillator illustrated in Fig. 1 is constructed in such a form wherein one terminal of the MOS construction type capacitance element 3 is connected to the input terminal of the inverter amplifier 1. Therefore, as a result of this, to the other end of the MOS construction type capacitance element 3 there is applied a voltage whose level is Vcc/2 that represents the threshold level voltage Vref of the inverter amplifier 1.--

Please replace the last paragraph bridging pages 11 and 12 with the following rewritten paragraph:

--And, in a case where having supplied a direct current control voltage, whose level is from 0V to Vcc, to the control terminal Vcont, the terminal-to-terminal voltage of the MOS construction type capacitance element 3 varies within a range of from –Vcc/2 to Vcc/2 with the potential at a point of connection between the control terminal Vcont and the input terminal of

the inverter amplifier 1 operating as a basis. Therefore, resultantly, both a positive and a negative voltage are applied to the MOS construction type capacitance element 3 as was previously explained using Fig. 9, with the result that the capacitance value thereof varies over a wide range.--

Please replace page 12, first full paragraph, with the following rewritten paragraph:

A10 (cont'd)

--Namely, for example, in a case where the inverter amplifier 1 operates with a power supply voltage Vcc=5V, the one terminal of the MOS construction type capacitance element 3 is applied with the threshold voltage Vref of the inverter amplifier 1, whose level is Vref=2.5V. Further, at this time, when a control voltage (Vcont) falling within a range of from 0V to 5V is supplied to the control terminal Vcont as a positive voltage, the terminal voltage Vcont – Vref of the MOS construction type capacitance element 3 is controlled within a range of from –2. 5V to +2.5V. Therefore, it is possible to control the value of the capacitance over a wide range without using a minus power supply as in the conventional example.--

Please replace the last paragraph bridging pages 12 and 13 with the following rewritten paragraph:

--Namely, in the above-described construction, the MOS construction type capacitance element 3 is inserted into within a loop of oscillation. Therefore, to the terminal on the inverter amplifier 1 side of it, there is applied an alternating current voltage, operating as an oscillation signal, the intermediate voltage of that is the threshold voltage Vref whose level is Vref=2.5v.--

A11

Please replace page 13, first full paragraph, with the following rewritten paragraph:

--And, there is the phenomenon that the amplitude level of the alternating current voltage affects the sensitivity to variable capacitance of the MOS construction type capacitance element 3. By positively utilizing this property, it is possible to suppress the sensitivity to variable capacitance of the MOS construction type capacitance element 3 to an arbitrary value.--

Please replace page 13, third full paragraph, with the following rewritten paragraph:

A12

--Here, for better understanding of the matter, it is assumed that the relationship between the terminal-to-terminal voltage and the capacitance value of the MOS construction type

capacitance element be set such that, as illustrated in Figs. 2(a) and 2(b), the capacitance value varies in response to a control-voltage range of from –0.5V to +0.5V with the intra-terminal voltage of 0V as the center.--

p12 (cont'd)

Please replace the last paragraph bridging pages 13 and 14 with the following rewritten paragraph:

--In Fig. 2(a), the solid line A illustrates the relationship between the intra-terminal voltage and the value of the intra-terminal capacitance that holds true when a direct current voltage Vref = 2.5V, equal in level to the threshold voltage, is applied to one terminal of the MOS construction type capacitance element and a positive-polarity direct current control voltage about 2.5V as the center is applied to the other terminal of it. As seen, in a non-saturation region, in which the capacitance value linearly greatly varies, there is obtained a high sensitivity to variable capacitance of 80pF/V or so.--

Please replace page 14, first full paragraph, with the following rewritten paragraph:

--Regarding such MOS construction type capacitance element, under the assumption that the voltage Vref applied thereto be a bias voltage of 2.5V applied to the input terminal of the inverter amplifier 1, let's consider a case where that voltage Vref is an oscillation alternating current voltage, which varies about the center voltage of 2.5V, and which is fed back to the input end of the inverter amplifier 1.--

Please replace page 15, first full paragraph, with the following rewritten paragraph:

--On the other hand, when the amplitude level in the oscillation alternating current voltage is set to be an alternating current voltage C approximately equal to the width of the non-saturation voltage region as illustrated in Fig. 2(b), merely slightly decreasing the terminal-to-terminal voltage for example is followed by the arrival of the half cycles on the minus side of the alternating current voltage C at the saturation region. Therefore, the amount of change in capacitance that corresponds to the half cycles on the minus side in the region of the terminal-to-terminal voltage whose level is lower than that of such slightly decreased terminal-to-terminal voltage becomes small. Conversely, when making the level of the voltage Vcont higher than 0V, the MOS construction type capacitance element operates also similarly. Therefore, the

p13

A13 (cont'd) capacitance sensitivity to terminal-to-terminal's voltage becomes wide in range as indicated in dotted line C', namely widely varies with respect to the terminal-to-terminal voltage. Resultantly, it is possible to make the variable-capacitance sensitivity to 40pF/V.--

Please replace page 16, third full paragraph, with the following rewritten paragraph follows:

--The point at which the crystal oscillator illustrated in each of Figs. 3(a) and 3(b) differs from that illustrated in Fig. 1 is that the MOS construction type capacitance element 3 is inserted into between the crystal resonator 2 and the capacitor C1 or between the crystal resonator 2 and the capacitor C2. The circuit of Fig. 3(a) is constructed in such a form wherein one terminal of the MOS construction type capacitance element is connected to the output of the inverter amplifier 1 while the circuit of Fig. 3(b) is constructed in such a form wherein one terminal of the MOS construction type capacitance element is connected to the input of the inverter amplifier and the other terminal thereof is connected to the control terminal Vcont via a resistor R3.--

A14

Please replace the last paragraph bridging pages 16 and 17 with the following rewritten paragraph:

--Further, if as illustrated in Fig. 3(a) a fixed resistor or variable resistor Rc is inserted into between the point E in the circuit and the ground whereby the value of this resistor Rc is made arbitrarily settable, the voltage at the point E becomes controllable. As a result of this, the terminal-to-terminal's voltage of the MOS construction type capacitance element is controlled, which enables adjusting the frequency of the oscillation circuit.--

Please replace page 17, second full paragraph, with the following rewritten paragraph:

--The respect in which the crystal oscillator illustrated in Fig. 4 differs from those illustrated in Figs. 1, 3(a) and 3(b) is that the MOS construction type capacitance element 4 is inserted into between the crystal resonator 2 and the capacitor C1 and the MOS construction type capacitance element 5 is inserted into between the crystal resonator 2 and the capacitor C2. It is thereby arranged that either one of such MOS construction type capacitance elements has its one terminal connected to either one of the input and output terminals of the inverter amplifier 1 and has its other terminal connected to the control terminal Vcont via a resistor R3 or R4.--

A15

Please replace the last paragraph bridging pages 17 and 18 with the following rewritten paragraph:

--The respect in that the crystal oscillator illustrated in each of these figures is characterized is that the amplitude level of an alternating current voltage and a direct current bias voltage, which is a reference voltage, supplied to the MOS construction type capacitance element 3, are made respectively separately adjustable.--

Please replace page 18, first full paragraph, with the following rewritten paragraph:

--Namely, the crystal oscillator is constructed as follows. As illustrated in each of those figures, the MOS construction type capacitance element 3 is inserted between the crystal resonator 2 and the capacitor C1 or between the crystal resonator 2 and the capacitor C2. A central point of connection between the crystal resonator 2 and the MOS construction type capacitance element 3 is connected to the control terminal Vcont via a resistor R3. Further, the other terminal of the MOS construction type capacitance element 3 is connected to a central point of connection in a series circuit of a resistor R5 and a resistor R6, which is connected between a power supply Vcc and the ground. On the other hand, said other terminal of the MOS construction type capacitance element 3, as illustrated in (a) of the figures, is connected to an output side of the inverter amplifier 1 and, as illustrated in (b) of the figures, is connected to an input side of the inverter amplifier 1, via a series circuit of a resistor R2 and a capacitor C4.--

Please replace the last paragraph bridging pages 18 and 19 with the following rewritten paragraph:

--And, by constructing the circuit like that, initially, according to the relational expression of Vref (DC) = R6×Vcc / (R5 + R6), setting is performed of the reference voltage value Vref for the direct current bias voltage applied to the MOS construction type capacitance element 3 to thereby adjust the reference capacitance value of this element 3. Thereafter, according to the relational expression of Vref (AC) = R5×R6 ×V0 / ((R5 + R6)×(R2 + R5×R6 / (R5 + R6)), adjustment is performed of only the resistance value alone of the resistor R2. Setting is thereby performed of the amplitude of the alternating current voltage supplied to the MOS construction type capacitance element 3. If thereby adjusting the sensitivity to capacitance of the MOS construction type capacitance element 3, this adjusting of the sensitivity to capacitance has no